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REMARKS

I. Status of the Application

Claims 14-21 are pending in this application. In the November 16, 2005 office action, the Examiner rejected claims 14-21 under 35 U.S.C. § 103(a), as allegedly being unpatentable over U.S. Patent No. 5,094,956 to Ozaki et al. (hereinafter "Ozaki") in view of U.S. Patent No. 5,573,980 to Yoo (hereinafter "Yoo"). In this response, the Applicant traverses the examiner's rejection under 35 U.S.C. § 103(a).

II. The Examiner's Rejection of Claim 14 Under 35 U.S.C. § 103(a) Should be WithdrawnA. Applicant's Claim 14

Applicant's claimed invention, as set forth in independent claim 14, is directed to a semiconductor device having a substrate, active areas, a gate, a first non-planar metallization level and a second planar metallization level. The active areas are formed within the substrate and include a source area and a drain area. A gate is disposed between the source area and the drain area and is insulated from the substrate by an oxide layer. The first non-planar metallization level is formed in the substrate in contact with the active areas. The first non-planar metallization level includes a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate. As shown in Fig. 2, the non-planar metallization level is labeled as structure 42.

The third portion of the non-planar metallization level includes (1) a portion that covers a side face of the gate facing the source area, (2) a portion covering a surface of the gate facing away from the substrate, and (3) a portion covering a part of a side face of the gate facing the

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drain area. The portion that covers the side face of the gate facing the drain area terminates at an end displaced from the substrate by a predetermined displacement. An example of this third portion is labeled as 42C in FIG. 2 and covers the side of the gate 20 facing the source 14, the surface of the gate 20 facing away from the substrate 10, and a part of the side of the gate 20 facing the drain 16. The end of the third portion by the drain 16 terminates above the substrate 10 at a predetermined displacement distance (see, e.g., FIGs. 2 and 4).

The planar metallization level is spaced apart from the first metallization level above the substrate and is connected to the second portion of the first metallization level via a through connection.

B. Ozaki

In the November 16, 2005 Office action, the Examiner stated that Ozaki does not disclose “the first non-planar metallization level having a third portion that includes a portion covering a part of a side face of the gate facing the drain area, the portion covering the side face of the gate facing the drain area terminating at an end displaced from the substrate by a predetermined displacement.” (See Office action, p. 3). Applicant agrees that Ozaki at least does not disclose the foregoing.

C. Yoo

In the November 16, 2005 Office action, the Examiner stated that Yoo discloses a semiconductor device including a first non-planar metallization level formed on a substrate. The Examiner also alleged that Yoo discloses a first non-planar metallization level including a third portion, “the third portion including a portion covering a side face of the gate facing the source

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area, a portion covering a surface of the gate facing away from the substrate, and a portion covering a part of the side face of the gate facing the drain area, the portion covering the side face of the gate facing the drain area terminating at an end displaced from the substrate by a predetermined displacement, as shown in Fig. 6.” (See Office action p. 3). The examiner further alleged that “the third portion covers the side face of the gate facing the drain area and terminates at an end displaced from the substrate by a predetermined displacement for the disclosed intended purpose of forming a low resistance interconnection to other areas of the substrate. (See Office action, pp. 3-4).

A careful reading of Yoo shows that Yoo discloses a method for forming silicided self-aligned contacts for memory cells. Yoo first discloses the known prior art in Figs. 1A-1D. According to the prior art to Yoo, a substrate 10 is provided having two drain areas 20 and one source area 22 formed in the substrate. Two gate portions 16, 28 are arranged between the source area and each of the drain areas. On top of this structure, a thin oxide layer 18 is provided by means of a lithographic process. The portion of the oxide layer covering the source area 22 is then removed to allow the subsequent formation of the contact. Next, a thin polysilicon layer 30 and a thin metal layer 32 are formed and the structure is heated to form a metal silicide 34 at the interface between the source region and the 22 and the metal layer 32/polysilicon layer 30 (see Yoo Fig. 1D). The remaining portions of the metal and the polysilicon are then etched away (see Yoo Col. 2, lines 23-28).

After disclosing the above prior art, Yoo discloses that a problem with the prior art approach is seen in the formation of polycide stringers or stray filaments of metal silicide which are difficult to remove (see Yoo col. 2, lines 23-28). Yoo proposes a solution to this problem through the use of a different approach for forming the silicide region. Figs. 2 and 3 of Yoo

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correspond substantially to Figs. 1A and 1B, which describe the prior art. However, instead of depositing two layers, only the polysilicon layer 30 is applied and structured such that the polysilicon layer 30 only remains in the region covering the source area 22 (see Fig. 5). In the following step, the metal layer 32 of titanium is applied over the entire structure (see Fig. 6). Then, a first rapid thermal annealing process is carried out to form titanium silicide 35, and the unreacted layer of titanium is etched away, yielding the structure shown in Fig. 7. By means of a second rapid thermal annealing process, the silicide is driven deeper into the common source 22 and the device is further processed to yield the structure shown in Fig. 8 of Yoo.

D. Ozaki in View of Yoo

It is respectfully submitted that the Examiner has failed to make a prima facie case of obviousness with respect to claim 14. In order to make a prima facie case of obviousness, "there must be some suggestion or motivation, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings." MPEP § 2143. In addition, "the prior art reference[s] ... must teach or suggest all the claim limitations." *Id.*

1. There is No Suggestion or Motivation to Modify or Combine the References

"There are three possible sources for a motivation to combine references: the nature of the problems to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998). Furthermore, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so

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found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. MPEP § 2143.01 (emphasis added).

In the November 16, 2005 Office action, the Examiner failed to establish a motivation for combining Ozaki and Yoo. Instead, on pages 2-3 of the Office action, the Examiner argued what is shown in Ozaki and Yoo. Then, on page 4 of the Office action, the Examiner simply stated that it would have been obvious for one of ordinary skill in the art at the time the invention was made to form the limitations of claim 14. Absent a clear analysis and rationale for combining references as set forth above in MPEP § 2143.01, the Examiner's conclusion that one of ordinary skill in the art would have found it obvious to combine the references is merely impermissible "hindsight." See *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998).

One reason the references are not properly combinable is that the nature of the problem to be solved is completely different from that of the present invention. As set forth above, Yoo is concerned with avoiding the formation of stray filaments of metal silicide in the formation of self-aligned silicide contacts (see Yoo col. 2, lines 23-28). On the other hand, the present invention is concerned with reducing the feedback capacity of a field effect transistor (see present application, pp. 10-12). Nothing in Yoo is concerned with the reduction of the feedback capacity in a field effect transistor. Thus, the nature of the problems to be solved do not provide a motivation for combining the references.

Moreover, the Examiner's conclusions with respect to Yoo are not consistent with a combination of Yoo and Ozaki. For example, on page 3 of the Office action, the Examiner states "Yoo discloses a semiconductor device that comprises ... a first non-planar metallization level formed on the substrate in contact with the active areas including a first portion connectable to the source area 22, a second portion connected to the drain area 20 and a third portion at least

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partially covering the gate ... as shown in Fig. 6" (emphasis added). Regarding this conclusion by the Examiner, Applicant notes that Fig. 6 does not show the finally processed semiconductor device, but shows an intermediate product in a state during the processing thereof. The final product is shown in Fig. 8 and the gate structure 16, 28 is covered by the dielectric layers 50 on both sides. In addition, a metal contact 44 is provided. However, no metallization level as defined in claim 14 is shown. Thus, a man of ordinary skill in the art would certainly not consider an intermediate process result, as shown in Fig. 6 of Yoo, in an attempt to solve the problem considered by the present invention. Instead, a person of ordinary skill in the art would look at the entire end structure of the prior art. Thus, the final product of Ozaki would not be combined with the intermediate product of Yoo (Fig. 6). Accordingly, one of ordinary skill in the art would derive no hint from Yoo of the inventive solution of the present application.

In addition to the above, another reason the references are not properly combinable is that there is no explicit or implicit reason provided for doing so in the Ozaki and Yoo references. Accordingly, the Examiner has failed to provide any specific disclosures in Ozaki or Yoo that would suggest a combination of the references.

As set forth above, the Examiner has not provided any suggestion or motivation for combining the Ozaki and Yoo references. Without providing such a suggestion or motivation in compliance with MPEP § 2143, the Examiner has failed to make a prima facie case of obviousness, and the Examiner's rejection should be withdrawn.

2. The References Do Not Teach or Suggest All Claim Limitations

In addition to the above, the Examiner has failed to make a prima facie case of obviousness under MPEP § 2143 because neither Ozaki nor Yoo teach or suggest all of the

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limitations of claim 14, either alone or in combination. *See* MPEP § 2143.03.

A first example of a limitation of claim 14 shown in neither Ozaki nor Yoo is that of a semiconductor device with “a first non-planar metallization level including a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate, the third portion including a portion covering a side face of the gate facing the source area, a portion covering a surface of the gate facing away from the substrate, and a portion covering a part of a side face of the gate facing the drain area, the portion covering the side face of the gate facing the drain area terminating at an end displaced from the substrate by a predetermined displacement.”

On page 3 of the November 16, 2006 Office action, the Examiner references Fig. 6 of Yoo as showing the above limitation. However, Fig. 6 of Yoo discloses no such limitation. In particular, Yoo does not disclose a metallization level having a third portion including “a portion covering a part of a side face of the gate facing the drain area, the portion covering the side face of the gate facing the drain area terminating at an end displaced from the substrate by a predetermined displacement.” While not clear from the Office action, it is assumed that the Examiner references metal layer 32 in Yoo as corresponding the metallization level of claim 14. However, this metal layer 32 in Yoo does not include “a portion covering a part of a side face of the gate facing the drain area, the portion covering the side face of the gate facing the drain area terminating at an end displaced from the substrate by a predetermined displacement” as required by claim 14. Although the Examiner suggests that Fig. 6 of Yoo shows this limitation, no such limitation is shown in Fig. 6, and the Examiner failed to provide a specific reference to this limitation in Yoo. Because the Examiner admitted in the November 16, 2005, Office action that this limitation was absent in Ozaki, and because the limitation is also not found in Yoo, it is

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respectfully submitted that the Examiner's has not made a prima facie case of obviousness with respect to claim 14.

In addition to the above, Yoo does not disclose other limitations the Examiner outlines for Yoo on page 3 of the November 16, 2005 Office action. For example, Yoo does not disclose "a second portion of the metallization level connected to the drain area," as required by claim 14. While not clear from the Office action, it is assumed that the Examiner references metal layer 32 in Yoo as corresponding the metallization level of claim 14. However, this metal layer 32 in Yoo does not have a portion connected to the drain area 20. Instead, Yoo discloses an oxide layer 18 connected to the drain area.

As set forth above, the Examiner has not made a prima facie case of obviousness in the November 16, 2005 Office action. In particular, there is no motivation to combine Ozaki and Yoo. Furthermore, neither Ozaki nor Yoo teach or suggest all of the limitations of claim 14. Accordingly, the Examiner has not made a prima facie case of obviousness, and the rejection of claim 14 should be withdrawn.

III. The Examiner's Rejection of Claims 15-21 Under 35 U.S.C. § 103(a) Should be Withdrawn

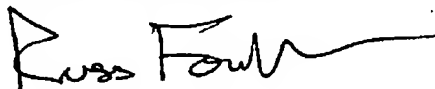
In the November 16, 2005 Office action, the Examiner rejected dependent claims 15-21 under 35 U.S.C. § 103(a). Each of these claims depends from and incorporates all of the limitations of one of independent claim 14. As set forth above, the examiner's rejection of claim 14 should be withdrawn. Therefore, because each of dependent claims 15-21 depend from and incorporate all of the limitations of claim 1, the Examiner's rejection of dependent claims 15-21 should also be withdrawn for at least the same reasons.

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IV. Conclusion

For all of the foregoing reasons, it is respectfully submitted the Applicant has made a patentable contribution to the art. Favorable reconsideration and allowance of this application is, therefore, respectfully requested.

Respectfully submitted,



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